A 60-GHz Transceiver on CMOS

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Abstract — Modern systems require transceivers that deliver gigabit speeds are smaller in size with lower power consumption and cost than existing technology consequently high speed transceivers operating at 60GHz and delivering multi-gigabit per second are receiving significant research interest. This paper describes a 60-GHz transmitter developed and tested on a 130-nm CMOS process.

Index Terms — CMOS, couplers, filters, millimeter wave circuit, mixer, power amplifier, RF, transmitter.

I. INTRODUCTION

Modern systems require wireless transceivers that are small, have low power consumption, low cost and deliver multi gigabit per second data rates. The authors (at NICTA) are producing an integrated wireless transceiver operating in the 60GHz ISM band delivering multi gigabit per second data rates. This paper provides an overview of the transceiver and performance of the fabricated components and challenges in implementing millimeter wave circuits on standard CMOS.

Advances in millimeter wave electronics have meant that significant portions of the system can now be integrated onto a single substrate or package. In order to achieve low cost and high digital integration CMOS process technology is utilised. CMOS is a standard and cost effective process for building digital circuits. Unfortunately when compared to more expensive processes such as Silicon Germanium (SiGe) and Gallium Arsenide (GaAs), CMOS has greater process variability, lower carrier mobility constants and smaller device breakdown voltages. This makes millimeter wave design, especially the design of Low Noise Amplifiers (LNA), Transmit Power Amplifiers (PA) and low phase noise Voltage Controlled Oscillators (VCOs) particularly challenging ([1]-[6]). However, the integration of these building blocks to construct a transceiver with suitable performance remains a challenge and few results have are available on integrated transceivers. This paper presents a 60-GHz transmitter implemented as a direct up-conversion architecture controlled and monitored by an on-chip digital calibration system to contend with process and temperature variation.

II. TRANSMITTER ARCHITECTURE

The transmitter presented in this paper is implemented as a direct conversion architecture. Fig. 1 illustrates the architecture of the integrated transmitter front end. The baseband differential signals from the I and Q channels are amplified by the variable gain amplifiers (VGAs) before being up-converted by the double balanced Gilbert cell mixers. The gain of the VGA is tuned to ensure sufficient output power. The gain of the VGA and digital calibration of each of the components is achieved by digital feedback control of the biasing voltages on each individual component of the transmitter. The biasing control of the transmitter is achieved by measuring variables such as power output, I and Q imbalance and using the 32 6-bit DACs to modify and control the biasing of the transmitter to ensure satisfactory performance.

The baseband signal is then directly converted to the 60-GHz RF signal by the I and Q mixers. These mixers are designed to be fully differential to achieve higher isolation between the LO and RF ports. The LO signal is in-band with the RF signal in this structure and any leakage of LO signal to the RF port degrades the receiver performance. Care has been taken with design and layout in the implementation of the transmitter chain to mitigate this issue.

The up-converted I and Q signals are combined through a meandering ring-hybrid coupler and then amplified by a five-stage Class-A power amplifier. Before transmission the RF signal is filtered by a band pass filter to ensure regulatory compliance. At millimeter-wave frequencies external bandpass filters are expensive and the transition from chip to printed circuit board mounted filters is very lossy. Therefore, an on-chip RF band-pass filter is designed and implemented. In the following sections III-V, we will give detailed descriptions on the constituent devices for the 60-GHz transmitter.

Fig. 1 Block diagram of the integrated 60GHz transmitter.
III. Up-conversion Mixer Design

The mixer employed in this transmitter is based on double-balanced Gilbert-cell structure. The Gilbert Cell structure is inherently immune to LO-to-RF feed through and has higher gain than the dual gate mixer [7]. The high LO-to-RF isolation is essential to maintaining low DC offset signals within the receiver and the higher gain facilitates the power amplifier to require less number of stages and consume less power as the gain per stage is small at this frequency. The simplified schematic is shown in Fig. 2. The design of up-conversion mixers involves the trade off between linearity, conversion gain and the rejection of the LO component at RF port. In order to achieve higher linearity, the lower transistors, M1 and M2 (2.5 μm × 40/0.12 μm), that serve as the transconductance stages are designed to be larger than the switching pairs M3 to M6 (2.5 μm × 10/0.12 μm). Although using larger width of switching pairs offers better switching performance and thus improves the noise figure performance, it makes the output matching network hard to tune and sensitive to process variation. The switching core consumes 15 mA current with a 1.6-V DC power supply.

TL1 to TL4 are four microstrip lines that are implemented to match the outputs to 50 Ω. A microstrip line is scalable in length and capable of accurately realizing small reactance values [1], [8]. The Q factor of microstrip line affects the gain and bandwidth of the mixer circuit as it affects the Q factor of the matching network. Since the performance of a microstrip line is affected by technology parameters such as metal layer conductivity and thickness as well as distance between signal and ground plane, microstrip lines with various layers for ground plane and signal path have been simulated in order to make tradeoff between the Q value and the inductance per unit length. The dimension of the up-conversion mixer is 200 μm × 500 μm.

IV. Power Amplifier Design

The power amplifier (PA) employed in this transmitter is a five-stage cascaded amplifier with each stage operating as a Class-A amplifier. The amplifier is shown in Fig. 3, with the input, output and inter-stage matching networks all integrated on-chip. A cascode topology was employed at each stage.

From computer aided design simulations, a transistor with gate length of 0.12 μm, finger width of 2.5 μm (to increase source-drain current and allow ease of matching), and 32 fingers per device for a total device size of 80 μm is chosen. The fmax for these transistors is greater than 135 GHz for a current density of 350 μA/μm of gate width.

V. Band-pass Filter and Coupler Design

A. RF Bandpass Filter on CMOS

The implemented filter is a 2nd-order microstrip rectangular open-loop bandpass filter. The 0° tapped feeding structure is used to introduce two transmission zeros at finite frequencies in the stopband, improving skirt selectivity. The filter is illustrated in Fig. 4(a). Its dimensions are optimized to minimize loss and size with the aid of the 3D full-wave EM simulator. The designed filter is built on the top thick aluminum metal layer with the ground plane on the bottom thin copper metal layer. Its size is only 415.5 μm × 502.8 μm (0.209 mm²).

When integrating the filter onto the 60-GHz transmitter, the high-impedance shielding technique presented in [9] is applied. This reduces the loss due to unwanted signal leakage to the silicon substrate through grid ground plane and also reduces the interference between components due to the unwanted coupling through the conductive substrate. This method is also employed in implementing the meandering ring-hybrid coupler and the meandering unfolded Lange coupler.

B. Compact 0°/180° coupler on CMOS

The designed meandering ring-hybrid coupler is a four port device. When driven at the differential-mode port its two outputs are out-of-phase by 180°. This can be used as a balun. When driven at the common-mode port its two outputs are in-phase so it behaves as a power divider/combiner. In a finite-
ground coplanar waveguide (FGCPW) configuration a phase inverter [10] is implemented by exchanging the signal and ground strips to provide a 180° shift. In order to further reduce the size meandering is used. Physical dimensions are derived with the aid of HFSS. The designed FGCPW meandering ring-hybrid coupler is built on top thick aluminum metal layer and is shown in Fig. 4(b). Its size is 325.35 μm × 325.35 μm (0.106 mm²). A CPW-to-microstrip transition was also designed when the designed ring-hybrid was connected to other components in the transmitter integration.

C. Compact 90° parallel coupled line coupler on CMOS

A meandering unfolded Lange coupler is designed as a quadrature coupler with 3 dB coupling ratios that provides two outputs with 90° phase difference and same amplitude from an LO input. With four parallel coupled lines to provide tight coupling, the unfolded Lange coupler can easily achieve 3 dB coupling ratio. In traditional design it is very difficult to fabricate necessary bonding wires to interconnect the lines of the coupler since they are very narrow and close together. In this design, thanks to the silicon multi-layer technology, these interconnections are easily implemented with vias and lower metal layers. The design was built on the thin aluminum metal layer to achieve high impedance. Meandering is also used to reduce the size. The designed meandering unfolded Lange coupler is shown in Fig. 4(c). It is only 121.24 μm × 111.02 μm (0.0135 mm²) in size.

VI. EXPERIMENTAL RESULTS

This 60-GHz transmitter design uses commercially available 130-nm CMOS technology. This standard CMOS technology offers transistors with f_t of 90 GHz and f_m of 140 GHz under appropriate biasing conditions. The microphotograph of the 60-GHz transmitter is shown in Fig. 5. The overall die size of the transmitter is 2 mm × 4.2 mm. The transmitter is tested via on-wafer probing.

The saturated power output at RF port for twenty (20) different transmitter chips received from the same multi project wafer (MPW). The LO input power was calibrated to be 4 dBm at LO pad for these measurements. Under process variation, an average P_{sat} of better than 3 dBm is achieved from 57 to 63 GHz. The control of RF output power is achieved by varying the VGA gain. By tuning the control voltage of the VGA from 180 to 600 mV, the RF power varies from -42 to 6 dBm. The LO-to-RF isolation for this transceiver is better than 27 dB from 57 to 65 GHz. The P_{1dB} and OIP3 of the 60-GHz transmitter is 2–dBm and 20.3–dBm respectively.

VII. CONCLUSIONS

In this paper an integrated 60-GHz transmitter implemented on IBM 8RF-DM 130-nm CMOS technology is presented. The results show that 130-nm CMOS has sufficient performance to implement an integrated radio at 60 GHz. The transmitter exhibits a $5 \pm 1.5$ dB measured $P_{sat}$ and LO-to-RF isolation of better than 27 dB from 57 to 65 GHz. Further more, the measured OIP1dB and OIP3 is 2 dBm and 20.3 dBm respectively which reflect a good linearity performance.

VII. ACKNOWLEDGEMENT

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REFERENCES

Fig. 5 Die micrograph of the integrated 60GHz transmitter