A Millimeter-Wave Phase Shifter on CMOS for Beamforming Applications

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Abstract

In this paper, a CMOS phase shifter is designed for beamforming applications operating in the millimeter-wave band from 50 to 70 GHz. Based on a synthesis transmission line structure, the phase shifter does not require a DC biasing current. Simulation results show that the phase shifter has a phase tuning range of 100° at 60 GHz. The input/output impedance of the phase shifter matches well with 50-Ohm source/load for a bandwidth of more than 80 GHz. At 60 GHz, the return loss is less than −15 dB and the insertion loss varies from 1.5 to 6.0 dB for as a function of control voltage. The phase shifter has a small footprint of 430 µm × 220 µm and can be easily extended to provide wider phase tuning range.

Keywords: millimeter-wave, phase shifter, variable delay line, CMOS

1 INTRODUCTION

Integrated phased-array antenna systems are gaining more and more interest during the last couple of years when researchers attempted to exploit the millimeter-wave band for high data-rate wireless transmission. The millimeter-wave band poses a significant challenge to designers because of its high path loss [1]. A solution to this problem is to use phased-array antenna systems which can provide high gain. However, the millimeter-wave band has a unique advantage over the low-frequency bands because of its very short wavelength. The short wavelength allows efficient antennae to now be built in a small form factor. As a result, an integrated solution in which the completed phased-array antenna system and the wireless transceiver is built on the same piece of semiconductor material becomes possible. To achieve a low-cost solution, such integrated solutions must be based on silicon semiconductor technology such as CMOS and BiCMOS.

One of the key components of a phased-array is the delay element, this is usually realized as a phase shifter in narrow-band systems [2]. A recent study has shown that integrated phased arrays operating at 60 GHz can be built on a low-cost CMOS process [1]. In [1], a phase selector which could only provide a finite number of discrete phase shift values was implemented to demonstrate the beamforming concept. The finite discrete phase shift values in [1] allowed the antenna beam to only be pointed in discrete steps.

In this paper a phase shifter implemented as a variable delay line (VDL) [3]–[5] with continuous phase tuning capability is presented. This type of phase shifter increases the performance of the phased-array by allowing the beam to be pointed in a continuous manner. Compared to other types of phase shifters such as reflective type [6], [7], and vector modulator type [8], which are restricted to narrow-band operation the phase shifter presented here has a much wider bandwidth. This makes it more suitable to wide bandwidth applications in the millimeter-wave band. In this implementation the group delay variation of the phase shifter was measured to be a few pico-seconds across the 20 GHz bandwidth around 60 GHz. Also, by operating much as a passive structure, i.e. a transmission line, the phase shifter requires negligible static power to bias itself.
The design of the phase shifter is covered in Section II and simulation results are presented in Section III followed by conclusions in Section IV.

2 CIRCUIT DESIGN

2.1 Design of the phase shifter

The phase shifter which operates as a synthesis transmission line [3] is a cascade of several identical π-segments each constructed from one inductor and two capacitors as shown in Figure 1. The time delay introduced by the phase shifter can be varied by tuning the values of the inductors and/or the capacitors. As described in [4] the inductor values can be varied by using active inductors. However, active inductor approach requires high power consumption and complex circuitry which can be challenging to implement at high frequencies. In this design, only the capacitance was varied.

Each π-segment is optimized to provide a maximum phase tuning range, a minimum power loss, and an impedance match to a desired characteristic impedance. The first two objectives must be traded off between each other through changing the bias of the phase shifter during its operation. This will be discussed later. The third criterion must be met during the design process. A perfect impedance match can be obtained by choosing the nominal values of \( L \) and \( C \) that satisfy

\[
L = \frac{2CZ_0}{1 + (2\pi CZ_0)^2} \quad (1)
\]

where \( f \) is the operating frequency, \( Z_0 \) is the desired characteristic impedance of the line, typically 50-Ohm, and \( X_L \) and \( X_C \) are the reactance of the inductor and capacitor, respectively. As an example, a graph showing various values of \( L \) and \( C \) that satisfy (1) for \( f = 60 \) GHz and \( Z_0 = 50 \) Ohm is plotted in Figure 2. In this design \( L \) is chosen to be 66 pH, which can be obtained from a 200-µm microstrip line, and the average value of \( C \) is 27 fF, which is obtained from a varactor.

![Figure 2. Nominal values of \( C \) and \( L \) for a 50-Ohm π-segment at 60 GHz.](image)

Once the π-segment is designed, multiple instances of it can be cascaded to achieve the desired range of phase shift. In this design, a five-segment phase shifter is realized. If more π-segments are used, the phase shifter can provide wider phase shift range at the cost of higher insertion loss.

2.2 Design of the varactor

The IBM 0.13-µm CMOS 8RF process used in this work offers a NMOS accumulation-mode varactor which can be used in applications that require tunability such as VCO and phase shifter. The varactor is a NFET built in a \( n \)-well with its source and drain shorted together. A cross-section view of the NMOS varactor is shown in Figure 3(a).

![Figure 3. (a) A cross-section of a single-finger NMOS varactor and (b) a simplified model of the varactor.](image)
and source/drain terminals is dependent on several factors including:

- the p-substrate to n-well diode, \( D_{ps-nw} \),
- the substrate resistance, \( R_{sub} \),
- the fringing capacitance between the poly-silicon gate and the source/drain, \( C_f \),
- the resistance of the poly-silicon gate, \( R_{ps} \), and
- the series resistance of the n-well in depletion mode and the accumulation layer in accumulation mode, \( R_s \).

As shown in Figure 1, the gate of the varactor is biased to a fixed value \( V_g \), through a large resistor, \( R_{bias} \), while the control voltage is fed to its source/drain. By using bypass capacitors, \( C_{bypass} \), to suppress the effect of \( D_{ps-nw} \) and \( R_{sub} \), the performance of the varactor is dependent on three parasitic items, \( C_f \), \( R_{ps} \), and \( R_s \). These parasitic components are strongly layout dependent and impact the capacitance tuning ratio and the quality factor of the varactor. The capacitance tuning ratio which is the ratio between the maximum effective capacitance, \( C_{max} \), to the minimum effective capacitance, \( C_{min} \), of the varactor

\[
    r_C = \frac{C_{max}}{C_{min}} \tag{2}
\]

is reduced due to the bias-independent fringing capacitance, \( C_f \). The quality factor, \( Q \), is lowered by the resistance of the poly-silicon gate, \( R_{ps} \), and the series resistance, \( R_s \). It is important to have high \( r_C \) to obtain large phase tuning range from the \( \pi \)-segment [6]. It is also desired to reduce \( R_{ps} \) and \( R_s \) to increase \( Q \) to minimize the insertion loss of the circuit.

To maximize \( r_C \) and \( Q \), \( C_f \), \( R_{ps} \), and \( R_s \) need to be minimized. To reduce \( C_f \) the varactor should be laid out as a single finger device to minimize its perimeter. Where as to reduce \( R_{ps} \) and \( R_s \), the varactor should be laid out as many small fingers in parallel. The optimization process to reduce \( C_f \), \( R_{ps} \), and \( R_s \) results in a varactor with 18 fingers (6 rows × 3 columns) each 0.24-\( \mu \)m long and 1-\( \mu \)m wide. The \( C\)-V and \( Q\)-V characteristics of this varactor at 60 GHz are simulated and shown in Figure 4.

The biasing conditions also plays an important role to the performance of the varactor. Figure 4 shows that as \( V_{gs} \) exceeds 0 V, the rate of increase of the effective capacitance starts to decrease and the quality factor drops to below 10. The use of positive \( V_{gs} \) is, therefore, not effective since it results in a high loss without much phase variation. The extension of \( V_{gs} \) toward positive values, by decreasing \( V_{ctrl} \), will result in a wider phase tuning range, because \( r_C \) is increased, at the cost of more loss, because \( Q \) is decreased. In our simulation \( V_g \) is fixed at 0.7 V and \( V_{ctrl} \) is varied from a maximum of 1.2 V to a minimum of 0.5 V.

### 2.3 Layout considerations

Figure 5 shows the layout of the phase shifter embedded in a testing pad frame. The phase shifter consists of five \( \pi \)-segments in series. For testing purposes, two matching networks were added to the input and output of the phase shifter to tune out the pad capacitance. The entire layout occupies an area of 1000 \( \mu \)m × 450 \( \mu \)m while the phase shifter is only 430 \( \mu \)m × 220 \( \mu \)m.

As mentioned above, the 66-pH inductor of the \( \pi \)-segment was implemented as a 200-\( \mu \)m microstrip. This transmission line was constructed in a S-shape to make the \( \pi \)-segment compact and easy to cascade with each other. The phase shifter design is, therefore, extensible in the sense that it allows phase shifter with wider (or narrower) phase shift range to be constructed simply adding (or removing) some \( \pi \)-segments from the current design.

In this design, side shielding metal strips were added to the microstrip to prevent coupling between successive segments. Substrate shielding technique as described in [9] was also exercised throughout the design.

### 3 PERFORMANCE

The simulated return losses at different control voltages are shown in Figure 6. The return loss is below –10 dB for a wide bandwidth from 20 GHz to exceeding 100 GHz. This effect is expected as the phase shifter is based on a transmission line. Around 60 GHz, the return losses are below –20 dB, which indicates a very good impedance matching to 50-Ohm termination, for all control voltages of interest.
Figure 6. Measured return losses at different control voltages.

Figure 7(a) and (b) respectively show the variation of phase shift and insertion loss versus control voltage. Across the range of control voltage from 0.5 to 1.2 V, the amount of phase shift introduced by the phase shifter varies by 100 degrees and the insertion loss varies from 1.5 to 6.0 dB.

Figure 7. Variation of (a) phase shift and (b) insertion loss at different control voltages.

The group delay is plotted in Figure 8. The group delay variation is less than 4 ps within a 10-GHz bandwidth centered at 60 GHz. A constant group delay is crucial for handling wideband signals without introducing too much distortion.

Figure 8. Group delay of the phase shifter.

4 CONCLUSION

The design of a phase shifter on a CMOS process for the millimeter-wave band around 60 GHz has been presented. The phase shifter can provide 100° of phase tuning range at 60 GHz and a good impedance matching to 50-Ohm source/load. It also exhibits a flat group delay which is important for wideband operation. The phase shifter can be utilized in building phased-array system on CMOS for beam forming applications around 60 GHz.

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